IN THE SPECIFICATION

Please amend the paragraphs listed below to read as follows:

[0011] In accordance with this invention, ~~a method is provided for forming~~ an SOI MOSFET device with a silicon layer is formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon above a gate dielectric layer, which is formed on the surface of the silicon layer. A cap comprising an amorphous silicon layer is formed on the top surface of the gate polysilicon. A hard mask is formed on top of the cap. A notch is formed in the periphery of the cap layer. The notch is filled with a plug composed of a dielectric material between the gate electrode and the hard mask. The plug formed in the notch extends down below the level of the top of the sidewall spacers for the purpose of eliminating the exposure of the gate polysilicon ~~so that form ation~~ to avoid formation of spurious epitaxial growth during the formation of raised source/drain regions. ~~is avoided.~~

[0021] FIG. 2A shows the device 10 of FIG. 1A, which has been modified in accordance with this invention by forming an amorphous silicon cap layer 21 [[21B]] on the upper surface of the gate electrode 18 prior to forming the hard mask 22 on the top surface of the gate electrode 18, above the amorphous silicon layer. Then notches 24 (shown in FIGS. 3F and 3G) were formed at the top of the gate electrode 18 between the cap layer 21 and the gate electrode 18 by etching away the outer edges at the periphery of the amorphous silicon cap layer 21 [[21B]]. The notches 24 at the top of the gate electrode 18 were filled with dielectric plugs 26P thereby forming a Top Notched Gate (TNG) structure. The reason that the notches 24 were filled with the dielectric plug 26P was to prevent formation of the kinds of nodules $28T_2$ seen in FIG. $1B_2$ on the polysilicon at the upper end of the gate electrode 18.

[0023] FIG. 2A shows spacer pull-down of spacers 26S extending down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D. FIG. 2A shows the structure of the SOI device 10 in accordance with this invention, prior to epitaxial growth of the raised source/drain regions 28S/28D of FIG. 2B on the surface of the thin silicon layer 12 of the device 10. The device 10 includes a thin silicon layer 12 formed on a Buried OXide (BOX) layer 12. A gate electrode stack is formed on the thin silicon layer 12. The gate electrode stack includes a dielectric (gate oxide) layer 14 formed above the thin silicon layer 12; a gate electrode 18 composed of polysilicon above the gate dielectric layer 14; the notched amorphous silicon, cap layer 21 bordered by the dielectric plugs 26P formed on the upper surface the gate electrode 18; and the hard mask 22 covering the upper surfaces of the amorphous silicon, cap layer 21 and the upper surfaces of the dielectric plugs 26P. Sidewall spacers 26S composed of silicon oxide have been formed on the sidewalls of the gate electrode 18 which cover the sidewall surfaces of the gate electrode 18 entirely and which reach up high enough from the silicon layer 12 to overlap the edges of the dielectric plugs 26P. The amorphous silicon cap layer 21 and the dielectric plugs 26P are covered by the hard mask 22. In other words, the sidewall spacers 26S, which cover the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P, which fill the notches 24, as shown in FIGS. 3F and 3G. The dielectric plugs 26P are formed at the top of the gate electrode 18 by etching away the outer edges of amorphous silicon cap layer 21 thereby recessing the periphery of the amorphous silicon cap layer 21 as described below with reference to FIGS. 3H and 3I.

[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D. There is no spurious growth on the top corner of the poly-silicon of the gate electrode 18 of the kind seen in FIG. 1B adjacent to the dielectric plugs 26P. The tops of the sidewall spacers 26S, in addition to covering the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P

[0025] FIGS. 3A-3J illustrate the process flow to construct the structure of FIGS. 2A and 2B. One advantage of this method/structure of this invention is that there is very little processing required above the normal process flow. The key is to form a top notched gate structure (TNG) with notches 24 shown in FIGS. 3F and 3G which can then be filled as illustrated by FIGS. 3H and 3I with a set of dielectric plugs 26P during the normal process flow. The structure is formed using the following steps.

[0027] FIG. 3A shows a potential gate electrode stack comprising SOI material Buried OXide (BOX) layer 11 of silicon dioxide covered with a conventional SOI thin silicon layer 12. [[A]] First a blanket layer of gate oxide layer 14B was formed on the top surface of BOX layer 11. [[and]] Next, a blanket polysilicon layer 18B ~~have been~~ was formed [[over]] on the [[BOX]] top surface of gate oxide layer 14B. [[11.]] The blanket polysilicon layer 18B may be doped or undoped.

[0028] FIG. 3B shows the stack of FIG. 3A after the first step of the present invention leading to the formation of the Top Notched Gate (TNG) structure of this invention, which is to form a blanket, thin amorphous silicon cap layer 21B on the top surface of the polysilicon layer 18B [[in]] by the process of ion implantation of ions 21I into the top surface of the blanket polysilicon layer 18 for the gate electrode 18. Germanium or silicon ions (21I) are implanted to a dose sufficient to amorphize the desired thickness of polysilicon layer 18B. The thickness of the amorphous cap layer 21B can be tailored by the choice of ion energy used to implant the ions 21I.

[0029] FIG. 3C shows a process of gate patterning applied to the device 10 of FIG. 3B. This is done starting with the deposition [[over]] on the surface of the blanket amorphous silicon cap layer 21B of a blanket hard mask layer 22B composed of a hard mask material (e.g. silicon nitride, TEOS, etc) and then proceeding with the initial steps of photolithographic patterning by forming a photoresist (PR) mask 23 [[over]] on the blanket hard mask layer 22B.

[0032] FIG. 3F shows the device 10 of FIG. 3E after the TNG selective formation of the undercut notches 24 in the amorphous silicon cap layer 21B of FIG. 3E. [[as]] In this step the undercut notches 24 are formed below the outer edges of the hard mask 22 ~~to form~~ thereby forming a recessed amorphous silicon cap 21 between the notches 24 above the blanket gate electrode layer 18B. Selective undercut of the amorphized layer 21B to form the notched amorphous silicon cap 21 is done during polysilicon RIE (described in detail below). In other words, an RIE etching process removes the peripheral portion of the amorphous silicon cap layer 21B to form recesses 24 at the edges thereof producing the notched amorphous silicon cap 21 which remains intact between the notches 24 and below the hard mask 22 which remains intact as shown in FIGS. 3E and 3F.

[0033] FIG. 3G shows the device of FIG. 3F, with the TNG structure after anisotropic etching of the blanket polysilicon layer 18B and the blanket gate dielectric layer 14B by RIE to form the polysilicon gate electrode 18 and gate dielectric layer 14 aligned with hard mask 22. This is done with a standard RIE etch for selectively and anisotropically etching polysilicon aligned with respect to the hard mask 22.

[0034] FIG. 3H shows the device 10 of FIG. 3G after blanket deposition of a spacer layer 26B composed of an appropriate spacer material covering the surface of device 10 while at the same time it is filling the notches 24 [[in]] on the recessed edges of the amorphous silicon cap layer 21 [[21B]] with material which will provide the plugs 26P [[26B]] seen in FIGS. 2A, ~~and~~ 2B, 3I, and 3J. The spacer material [[in]] forming the spacer layer 26B ~~is composed of~~ comprises any spacer material such as a dielectric material, e.g. silicon oxide or silicon nitride.

[0035] FIG. 3I shows the device 10 of FIG. 3H after etching back the spacer layer 26B to form spacers 26S on the sidewalls of the gate electrode 18 and at the same time [[as]] to form protective, dielectric plugs 26P ~~are being formed~~ in the undercut notches 24 on the edges of the amorphous silicon cap layer 21 at the top of the gate structure, to provide for protection of the polysilicon of the gate electrode 18 during the subsequent formation of epitaxial raised source/drain regions 28S/28D ~~formation~~ shown by FIG. 3J.

[0036] FIG. 3J shows the device of FIG. 3I after formation of the raised source/drain regions 28S/28D juxtaposed with the sidewall spacers 26S with no nodules formed at the top of the gate electrode 18 adjacent to the protective, dielectric plugs 26P during the epitaxial process used to form raised source/drain regions 28S/28D. The problem that is illustrated by FIG. 1B has been overcome since there is no exposure of the upper corners of the gate electrode 18, so that there is no spurious growth of silicon nodules 28T. Thus the top corners of the gate electrode 18 are protected.

[0037] At this point the polysilicon sidewall spacers 26S and top cap 22 can be removed from above the amorphous silicon cap layer 21 and the protective, dielectric plugs 26P and conventional process steps, as known to those skilled in the art, can be applied to finish the formation of the FET structure.